



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/773,058

02/04/2004

Kayhan Kucukcakar

SYN-0513

5479

35273 7590 06/24/2008
BEVER, HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE, CA 95110

EXAMINER

PATEL, SHAMBHAVI K

ART UNIT

PAPER NUMBER

2128

MAIL DATE

DELIVERY MODE

06/24/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

1. This Office Action is in response to the Amendments/Remarks submitted 25 March 2008.
2. Claims 1-9, 12-19, 25, 27-30, 32-43, 45, 47-53, 55-62, 64-70, 72-78 and 83-96 have been presented for examination. Claims 83-96 are newly added.

Response to Arguments

3. In view of the cancellation of claims 20-24 and 79-80, the 35 U.S.C. 101 rejection is withdrawn.
4. Applicant's arguments with respect to the prior art rejection of claims 1-9, 11-30, 32-43 and 45-82 have been considered but are not persuasive. **Applicant submits**, on page 23 of the remarks, that neither Schulz nor Schultz disclose the amended limitation "analyzing the intermediate results to construct merged results, the merged results providing at least one of: what parts of the design have not been analyzed, whether the design has been exhaustively analyzed for a particular corner/mode, and whether the design has been exhaustively analyzed for all corners/modes". **Examiner notes** that Schultz teaches "The multipass timing analysis of step 204 comprises defining all of the corner cases for analysis in step 210, performing the static timing analysis for a particular corner case in step 212, saving the results in step 214 and running another corner case in step 216. If the corner cases are completed in step 216, a multipass analysis is performed in step 218 and saved in step 220." (**Schultz: [0032]**). The results of these passes are then saved, analyzed and merged (**[0033]**). Because the merged results are not produced until all of the corners are analyzed, the merged results provide that the design has been exhaustively analyzed for a/all corner(s)/mode(s).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 83-96 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding **claim 83**, it is unclear what the term "for each path" means. The intermediate results are performed on the design,

Art Unit: 2128

and it is unclear how these results are analyzed to create merged results that contain paths. All other claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-9, 12-19, 25, 27-30, 32-43, 45, 47-53, 55-62, 64-70, 72-78 and 83-96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schultz (US Pub. No. 2004/0044976) in view of Schulz ('Focus Report: Timing Analysis' 2000).**

Regarding claims 1, 25, 45 and 62:

Schultz discloses a method of performing static timing analysis on a design, the method comprising:

- a. performing multiple static timing analysis runs with the design, each run using a predetermined set of parameters including a plurality of corners ([0025]; [0032] **multipass timing analysis defines all the corner cases for analysis and performing the static timing analysis for each corner case**).
- b. saving intermediate results from the multiple static timing analysis runs ([0032] **the results from each run are saved in step 214**)
- c. analyzing the intermediate results to construct merged results ([0027]-[0029]; [0033] **multipass analysis performed on saved results**) providing at least whether the design has been exhaustively analyzed for a particular/all corners ([0032] **the results are merged only after all of the specified corners are analyzed**)

Regarding **claim 25, Schultz discloses** software tools containing instructions to perform the above steps ([0024]).

Regarding **claim 62, Schultz teaches** reporting parts of the design that are analyzed for each corner as well as for those not (**Schultz: [0040]: all results can be accessed**).

Schultz does not explicitly disclose performing multiple static analysis runs for a plurality of modes. **Schulz teaches** performing multiple static analysis runs for a plurality of modes (**Schulz: “Under the Hood” 5th paragraph**). At the time of the invention, it would have been obvious to one of ordinary skill in the arts to combine the teachings of Schulz and Schultz in order to isolate troublesome areas in full-chip analysis and to verify timing passing through test logic (**Schulz: “Under the Hood” 5th paragraph**).

Regarding claims 3, 27, 47, 64:

Schultz discloses sharing information within the multiple static timing analysis runs ([0024]). The analysis are run on the same circuit schematic but with different parameters.

Regarding claims 4, 28, 48, 65:

Schulz teaches performing the multiple static timing analysis runs in parallel (**‘Putting Timing Analysis Tools to Work’ 7th paragraph**). The prior art discloses single-pass analysis of best/worst case conditions in order to minimize cycle time.

Regarding claims 5, 29, 49, 66:

Schultz discloses performing the multiple static timing analysis runs in series (**figures 2-5**).

Regarding claims 6, 30, 35, 50 and 67:

Schultz discloses forming a database of intermediate results that can be queried at different levels of detail ([0040]).

Regarding claims 7, 36, 51 and 68:

Schultz discloses restoring (i.e. reading) the database and making additional queries ([0040]).

Regarding claims 8, 37, 52 and 69:

Schultz discloses querying from one or more runs ([0040]).

Regarding claims 9, 38, 53 and 70:

Schultz discloses adding additional results to the saved results of each run during each query ([0032], [0033]).

Regarding claims 12-13, 39-40, 55-56, 72-73:

Schultz discloses saving intermediate results that can be arbitrarily queried and include a predetermined set of parameters that are used in creating additional results ([0032], [0033]).

Regarding claims 14, 41, 57, 74:

Schultz discloses the method of claim 1, wherein the saved results include results of predetermined queries ([0032]).

Regarding claims 15, 42, 58, 75:

Schultz discloses the method of claim 1, wherein the saved results include design corner description ([0026]) and timing delay ([0044]).

Regarding claims 16, 43, 59, 76:

Schultz discloses reporting the merged results including design corner description and timing information ([0026]) and timing delay ([0044]).

Regarding claims 17, 32, 60, 77:

Schulz teaches allowing multiple modes and corners to be analyzed simultaneously (**‘Putting Timing Analysis Tools to Work’ 7th paragraph**). The prior art discloses single-pass analysis of best/worst case conditions in order to minimize cycle time.

Regarding claims 18, 61, 78:

Schulz teaches modifying a predetermined set of parameters after completing an initial multi-mode/multi-corner analysis, and performing an analysis to provide a what-if capability (**‘More Bells and Whistles’ 2nd paragraph**).

Regarding claim 19:

Schultz discloses a method of performing static timing analysis on a design, the method comprising:

- a. performing multiple static timing analysis runs with the design, each run using a predetermined set of parameters including a plurality of corners ([0025]; [0032] **multipass timing analysis defines all the corner cases for analysis and performing the static timing analysis for each corner case**).
- b. saving intermediate results from the multiple static timing analysis runs ([0032] **the results from each run are saved in step 214**)
- c. analyzing the intermediate results to construct merged results wherein desired information is merged first ([0027]-[0029]; [0033] **multipass analysis performed on saved results**) providing at least whether the design has been exhaustively analyzed for a particular/all corners ([0032] **the results are merged after all of the specified corners are analyzed**)

Schultz does not explicitly disclose performing multiple static analysis runs for a plurality of modes.

Schulz teaches performing multiple static analysis runs for a plurality of modes (**Schulz: “Under the Hood” 5th paragraph**). At the time of the invention, it would have been obvious to one of ordinary skill in the arts to combine the teachings of Schulz and Schultz in order to isolate troublesome areas in full-chip analysis and to verify timing passing through test logic (**Schulz: “Under the Hood” 5th paragraph**).

Art Unit: 2128

Regarding claim 33:

Schultz discloses a computer-readable medium comprising instructions, that when executed by a processor, provide instructions for generating merged results from multiple static timing analysis runs, the instructions comprising:

- a. a first set of instructions for performing multiple static timing analysis runs with the design, each run using a predetermined set of parameters including a plurality of corner ([0025]; [0032] **multipass timing analysis defines all the corner cases for analysis and performing the static timing analysis for each corner case**).
- b. a second set of instructions for saving intermediate results from the multiple static timing analysis runs ([0032] **the results from each run are saved in step 214**)
- c. a third set of instructions for analyzing the intermediate results to construct merged results ([0027]-[0029]; [0033] **multipass analysis performed on saved results**) providing at least whether the design has been exhaustively analyzed for a particular/all corners ([0032] **the results are merged only after all of the specified corners are analyzed**)

Schultz does not explicitly disclose performing multiple static analysis runs for a plurality of modes.

Schulz teaches performing multiple static analysis runs for a plurality of modes (**Schulz: “Under the Hood” 5th paragraph**). At the time of the invention, it would have been obvious to one of ordinary skill in the arts to combine the teachings of Schulz and Schultz in order to isolate troublesome areas in full-chip analysis and to verify timing passing through test logic (**Schulz: “Under the Hood” 5th paragraph**).

Regarding claim 34:

Schultz discloses a computer-readable medium comprising instructions, that when executed by a processor, provide instructions for generating merged results from multiple static timing analysis runs, the instructions comprising:

- d. a first set of instructions for performing multiple static timing analysis runs with the design, each run using a predetermined set of parameters including a plurality of corner ([0025]; [0032]

multipass timing analysis defines all the corner cases for analysis and performing the static timing analysis for each corner case).

- e. a second set of instructions for saving intermediate results from the multiple static timing analysis runs **([0032] the results from each run are saved in step 214)**
- f. a third set of instructions for analyzing the intermediate results to construct merged results **([0027]-[0029]; [0033] multipass analysis performed on saved results)** to provide analysis coverage and path information at multiple levels of detail **([0040])**
- g. reporting the merged results, providing at least whether the design has been exhaustively analyzed for a particular/all corners **([0032] the results are merged only after all of the specified corners are analyzed)**

Schultz does not explicitly disclose performing multiple static analysis runs for a plurality of modes.

Schulz teaches performing multiple static analysis runs for a plurality of modes **(Schulz: “Under the Hood” 5th paragraph)**. At the time of the invention, it would have been obvious to one of ordinary skill in the arts to combine the teachings of Schulz and Schultz in order to isolate troublesome areas in full-chip analysis and to verify timing passing through test logic **(Schulz: “Under the Hood” 5th paragraph)**.

Regarding claim 41:

Schulz discloses saving results of predetermined queries **(‘A Look Under the Hood’ 2nd paragraph)**. If the engine calculates slack and constraints violations, the reports containing this data are then presented to the user.

Regarding claim 42:

Schulz discloses saving cell delays, net delays, transition times, path reports, bottleneck reports, modes, slack, and constraints **(‘An Introduction Please’ 2nd paragraph; ‘A Look Under the Hood’ 2nd, 5th-6th paragraphs; ‘Putting Timing Analysis Tools to Work’ 9th paragraph)**.

Regarding claim 43:

Schulz discloses reporting the merged results including cell delays, net delays, transition times, path reports, bottleneck reports, modes, slack, and constraints (**‘An Introduction Please’ 2nd paragraph; ‘A Look Under the Hood’ 2nd, 5th-6th paragraphs; ‘Putting Timing Analysis Tools to Work’ 9th paragraph**).

7. **Claims 83-96 are rejected under 35 U.S.C. 103(a)** as being unpatentable over **Schulz (‘Focus Report: Timing Analysis’ 2000)** in view of **Schultz (US Pub. No. 2004/0044976)** in view of **Ernst (“Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation”)**.

Regarding claim 83:

Schulz discloses a method of performing static timing analysis on a design, the method comprising:

- a. performing multiple static timing analysis runs with the design, each run using a predetermined set of parameters including a mode and corner (**‘A Look Under the Hood’ 5th paragraph**). The prior art discloses tools that are capable of performing minimum/maximum delay analysis (i.e. multiple runs are needed, one to account for the minimum delay and a second to account for the maximum delay) and modal analysis.
- b. saving intermediate results from the multiple static timing analysis runs (**‘A Look Under the Hood’, 2nd paragraph**). Once the runs are completed, the data is collected and presented to the user in reports and various visualization tools.
- c. analyzing the results to determine timing violations (**Introduction: 2nd paragraph**)

Schulz does not explicitly disclose merging the results. **Schultz teaches** merging the results to provide analysis coverage (**Schultz: [0029]**). At the time of the invention, it would have been obvious to one of ordinary skill in the arts to combine the teachings of Schulz and Schultz in order to minimize the number of probe points necessary to isolate a failure and eliminate manual tracking of schematic and waveforms during root cause debugging (**Schultz: [0011]**). **Schulz and Schultz do not teach** calculating the percentage of times that timing violations exist for all analyzed modes and corners. **Ernst teaches** performing timing analysis (**Ernst: Introduction**), including calculating the timing error rates (**Ernst: section 2**). At the time of the invention, it would

Art Unit: 2128

have been obvious to one of ordinary skill in the art to combine the teachings of Schulz, Schultz, and Ernst in order to provide *in-situ* monitoring of the actual circuit delay (**Ernst: Introduction**).

Regarding claim 84:

Schulz teaches performing the multiple static timing analysis runs in parallel (**‘Putting Timing Analysis Tools to Work’ 7th paragraph**). The prior art discloses single-pass analysis of best/worst case conditions in order to minimize cycle time.

Regarding claim 85:

Schultz discloses performing the multiple static timing analysis runs in series (**figures 2-5**).

Regarding claim 86:

Schultz discloses forming a database of intermediate results that can be queried at different levels of detail ([0040]).

Regarding claim 87:

Schultz discloses restoring (i.e. reading) the database and making additional queries ([0040]).

Regarding claim 88:

Schultz discloses querying from one or more runs ([0040]).

Regarding claim 89:

Schultz discloses adding additional results to the saved results of each run during each query ([0032], [0033]).

Regarding claims 90 and 91:

Schultz discloses saving intermediate results that can be arbitrarily queried and include a predetermined set of parameters that are used in creating additional results ([0032], [0033]).

Regarding claim 92:

Schultz discloses the method of claim 1, wherein the saved intermediate results include results of predetermined queries ([0032]).

Regarding claim 93:

Schultz discloses the method of claim 1, wherein the saved results include design corner description ([0026]) and timing delay ([0044]).

Regarding claim 94:

Schultz discloses reporting the merged results including design corner description and timing information ([0026]) and timing delay ([0044]).

Regarding claim 95:

Schulz teaches allowing multiple modes and corners to be analyzed simultaneously (**‘Putting Timing Analysis Tools to Work’ 7th paragraph**). The prior art discloses single-pass analysis of best/worst case conditions in order to minimize cycle time.

Regarding claim 96:

Schulz teaches modifying a predetermined set of parameters after completing an initial multi-mode/multi-corner analysis, and performing an analysis to provide a what-if capability (**‘More Bells and Whistles’ 2nd paragraph**).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Examiner's Remarks: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

Application/Control Number: 10/773,058
Art Unit: 2128

Page 13

SKP